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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

INVENTOR:	Haswell et al.	EXAMINER:	Mujtaba M. Chaudry
SERIAL NO.:	10/604,141	ART UNIT:	2133
FILING DATE:	June 27, 2003	DATE:	November 20, 2006
FOR:	Method and System for Optimized Instruction Fetch to Protect Against Soft and Hard Errors		

RESPONSE AFTER FINAL

Mail Stop _____
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is responsive to the Office Action mailed September 19, 2006 finally rejecting the instant application.

Claims 1-20 stand finally rejected under 35 USC § 103 as being obvious from Sakamoto U.S. Patent No. 4,617,660 in view of Albonesi U.S. Patent No. 4,920,539. Applicants again respectfully traverse this rejection.

The Examiner continues to correctly state that "Sakamoto does not explicitly teach to check the data signal for corruption at the time it is received by the computer processor as stated in the present application." Office action, p.5. However, not only does Sakamoto not

teach this, he explicitly teaches against checking the data signal for corruption at the time it is received by the computer processor:

> Under a normal operation mode, *the CPU first receives read data from the MU and executes a process using the received read data before detection and correction of an error in the read data, without waiting for the result of the error detection*. When an error is detected in the read data, the process by the CPU is stopped in response to a memory error signal S_b, and then corrected data is written back in the memory. Thereafter, the read-out operation from the memory is retried. Thus, the access time can be shortened, and high speed processing can be executed.

Sakamoto, column 4, lines 31-41 (emphasis added). Thus, it is clear that Sakamoto teaches that the processor should execute the process using the read data before detecting and correcting any error in that data. This is substantially different from the claimed invention in that Sakamoto's method allows processing to proceed with faulty data for some time.

Sakamoto's approach can be particularly problematic when, for example, the data is actually an instruction and the CPU executes the wrong instruction or perhaps attempts to execute an invalid instruction. An invalid instruction might also cause the CPU to grind to a halt before it is stopped by the memory error signal. Sakamoto teaches that recovery from an error involves stopping the processor, and retrying once the data has been corrected. In order to do so, the system must have the capability to re-create the exact state of CPU operations prior to the error, even after is has proceeded for some time using corrupted data. Such a capability can be rather costly in terms of additional logic, memory, registers, and the like, and difficult to implement in today's pipelined processors. It is therefore a unique advantage of the present invention to swap in a legal instruction as taught in the instant application. The processor will then never be required to execute an invalid or incorrect instruction, nor will it be required to stop processing. Instead, it will jump to an error handling routine, which will

cause the corrected data to be retrieved once it is available, and may also include the ability to process another task in the interim.

The Examiner has not taken issue with or contested the fact that Sakamoto's method teaches away from checking a data signal for corruption at the time it is received by the computer processor, as stated in the present application. More importantly, the Examiner has not provided a motivation that one of ordinary skill in the art would have to use an opposite approach, as the Examiner contends is taught by Albonesi.

The Examiner continues to cite the Albonesi patent for the error correction that goes against the teaching of Sakamoto, citing the passage at column 8, lines 11-29 referring to the correction of memory errors by detecting data error while the data is being transferred from memory to the system bus and generating corresponding corrected data if a data error is detected. The cited passage is in the claims of the Albonesi patent. Accordingly, one must read the Albonesi specification to understand what is meant by the cited claim passage. See *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 34 USPQ2d 1321, 1329 (Fed. Cir. 1995) (en banc), *aff'd*, 517 U.S. 370, 38 USPQ2d 1461 (1996) ("Claims must be read in view of specification, of which they are a part.") (citing *Autogiro Co. of America v. United States*, 384 F.2d 391, 397, 155 USPQ 697, 702 (Ct. Cl. 1967)).

With this in mind, a careful reading of the Albonesi specification makes it clear that Albonesi does not disclose or suggest "substituting the raw data signal with a predetermined reserved data signal and transmitting the predetermined reserved signal to the computer processor" as applicants claim. Albonesi states that "it is an object of the present invention to provide an improved system for memory error correction and, in particular, for correction of alpha particle type (soft) memory failures. Another object of the present invention is to provide a memory error correction system for use in a system wherein the various processors

employ writeback caches." Albonesi, column 1, lines 57-64. What Albonesi describes is basic, long-known error correction code (ECC) function, with a write-back of corrected data to memory. In Albonesi's method, the destination of the data must wait for the correction to take place before receiving the data. Albonesi does not address the problem whereby a processor cannot wait for the ECC logic to correct the error. If a fast processor were the destination in the Albonesi case, the processor would have to pause until the ECC correction was complete. This is referred to as "starving the processor" and is generally undesirable. Moreover, it is not what applicants claim in the instant invention. Accordingly, the broad interpretation by the Examiner made by reading only the cited claim passage in Albonesi is not supported or taught by a reading of the Albonesi patent as a whole.

The instant invention resolves this problem by reacting to the initial error detection signal, available before the corrected data. When an error is indicated, a predetermined reserved data signal is given to the processor in place of the corrupted data. This allows the processor to proceed with a valid instruction, even though there had been an error. In the meantime the data may be corrected and stored for subsequent processing. The system using the instant invention therefore can take advantage of the fact that a valid instruction will always be given to the processor without an ECC delay (regardless of whether or not there was an error), and can operate at a higher performance level. Only after the reserved data signal has been processed does the data correction occur in applicants' invention, as set forth in dependent claims 2-5, 12 and 17-19.

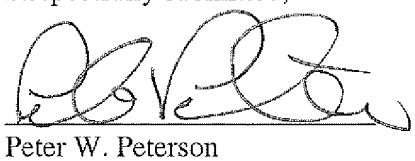
Accordingly, in order to combine the teachings of Sakamoto and Albonesi in the manner hypothesized, one of ordinary skill in the art would have to ignore the clear and direct teachings of Sakamoto that the processor "executes a process using the received read data before detection and correction of an error in the read data, without waiting for the result of

the error detection." Sakamoto, column 4, lines 31-41. There is no motivation given in either reference for proceeding against such a teaching. However, even if one did ignore Sakamoto's teaching in this regard, the Albonesi method would still not arrive at or suggest applicants' invention because the processor would have to wait for corrected data to proceed, and would not "substitut[e] the raw data signal with a predetermined reserved data signal and transmit[ ] the predetermined reserved signal to the computer processor" for processing as in applicants' invention. Thus, the hypothetical combination of Sakamoto and Albonesi does not render applicants' invention *prima facie* obvious.

Further, in applicants' preferred embodiment as recited in claims 6 and 13, the steps of transmitting the raw data signal from the data memory to a computer processor, simultaneously checking the raw data signal for data corruption, and transmitting either the raw or predetermined reserved signal to the computer processor are performed within a clock cycle. Such operations are nowhere disclosed or suggested in either Sakamoto or Albonesi. The Examiner's final rejection does not refute that applicants' invention of claims 6 and 13 is not obvious from the cited art.

It is respectfully submitted that the application is in a condition where allowance of the entire case is proper. Reconsideration and issuance of a notice of allowance are respectfully solicited.

Respectfully submitted,



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